CLAIMS:

1. A radiation detector, comprising:

a detection member including a plurality of pixels and configured to generate a first charge;

a first driver configured to supply the detection member with a first predetermined voltage so that the detection member generates the first charge;

an integration amplifier configured to amplify the first charge generated from the detection member; and

a first adjustment member provided in between the detection member and the integration amplifier, and configured to adjust an offset component included in the first charge to be amplified by the integration amplifier.

2. The detector according to claim 1, wherein the offset component is a charge generated from the detection element when a radiation is not radiated to the detector.

3. The detector according to claim 1, wherein the offset component is a charge output from the integration amplifier when a radiation is not radiated to the detector.

4. The detector according to claim 1, wherein the first adjustment member reduces the offset component.

5. The detector according to claim 1, wherein each of the plurality of pixels of the detection member includes a conversion element configured to convert a radiation to the first charge, a first capacitor configured to store the first charge converted by the conversion element, and a first switching element configured to generate the first charge stored in the first capacitor in response to the supply of the first predetermined voltage from the first driver.

6. The detector according to claim 5, wherein the first switching element comprises a thin film transistor.

7. The detector according to claim 1, wherein the first adjustment member is formed on a substrate where the detection member is formed.

8. The detector according to claim 1, wherein the first adjustment member includes a second switching element.

9. The detector according to claim 8, wherein the second switching element comprises a thin film transistor.

10. The detector according to claim 9, wherein a terminal of the thin film transistor is connected to a second capacitor.

11. The detector according to claim 9, wherein a terminal of the thin film transistor is grounded.

12. The detector according to claim 9, wherein a terminal of the thin film transistor is maintained at a predetermined potential.

13. The detector according to claim 9, wherein a terminal of the thin film transistor is open.

14. The detector according to claim 1, wherein the first adjustment member has a predetermined capacitance.

15. The detector according to claim 14, wherein the predetermined capacitance is a parasitic capacitance.

16. The detector according to claim 15, wherein, when the detection member generates the first charge through a signal line and the first adjustment member includes a first adjustment line, the parasitic capacitance is generated at a crossing point between the signal line and the first adjustment line.

17. The detector according to claim 16, wherein the signal line has a different width at the crossing point.

18. The detector according to claim 16, wherein the first adjustment line has a different width at the crossing point.

19. The detector according to claim 16, wherein the first adjustment line has a wider width than the signal line.

20. The detector according to claim 16, wherein, when the first adjustment member includes a plurality of first adjustment lines, the parasitic capacitance is generated at crossing points between the signal line and the plurality of first adjustment lines.

21. The detector according to claim 1, wherein, when the integration amplifier comprises a plurality of amplifying elements, the first adjustment member adjusts the offset component for each of the plurality of amplifying elements independently.

22. The detector according to claim 1, wherein, when the detection member generates the first charge through a plurality of signal lines, the first adjustment member adjusts the offset component for each predetermined number of the plurality of signal lines independently.

23. The detector according to claim 22, further comprising a pad configured to bundle the each predetermined number of the plurality of signal lines.

24. The detector according to claim 23, further comprising a tab configured to include the pad, wherein the integration amplifier is included in the tab and wherein the each predetermined number of the plurality of signal lines are connected to the integration amplifier through the pad.

25. The detector according to claim 23, wherein the first adjustment member includes a first adjustment line distributed along a left side of the each predetermined number of the plurality of signal lines, the first adjustment line extending to intersect the each predetermined number of the plurality of signal lines.

26. The detector according to claim 23, wherein the first adjustment member includes a first adjustment line distributed along a right side of the each predetermined number of the plurality of signal lines, the first adjustment line extending to intersect the each predetermined number of the plurality of signal lines.

27. The detector according to claim 23, wherein the first adjustment member includes a first adjustment line distributed along a left side of the each predetermined number of the plurality of signal lines, extending to intersect the each predetermined number of the plurality of signal lines, and further distributed along a right side of the each predetermined number of the plurality of signal lines.

28. The detector according to claim 23, wherein the first adjustment member includes a first adjustment line intersecting, near the pad, the each predetermined number of the plurality of signal lines.

29. The detector according to claim 1, further comprising a second adjustment member, provided in between the detection member and the integration amplifier, and configured to reduce a second charge resulting from the first predetermined voltage supplied to the detection member from the first driver, the second charge being included in the first charge to be amplified by the integration amplifier.

30. The detector according to claim 29, wherein the second adjustment member is formed on a substrate where the detection member is formed.

31. The detector according to claim 29, wherein the second adjustment member includes a third switching element.

32. The detector according to claim 31, wherein the third switching element comprises a thin film transistor.

33. The detector according to claim 32, wherein a terminal of the thin film transistor is connected to a third capacitor.

34. The detector according to claim 32, wherein a terminal of the thin film transistor is grounded.

35. The detector according to claim 32, wherein a terminal of the thin film transistor is maintained at a predetermined potential.

36. The detector according to claim 32, wherein a terminal of the thin film transistor is open.

37. The detector according to claim 29, wherein the second adjustment member has a predetermined capacitance.

38. The detector according to claim 37, wherein the predetermined capacitance is a parasitic capacitance.

39. The detector according to claim 38, wherein, when the detection member generates the first charge through a signal line and the second adjustment member includes a second adjustment line, the parasitic capacitance is generated at a crossing point between the signal line and the second adjustment line.

40. The detector according to claim 29, wherein the first adjustment member is provided between the detection member and the second adjustment member.

41. The detector according to claim 29, wherein the first adjustment member is provided between the second adjustment member and the integration amplifier.

42. The detector according to claim 1, wherein the first adjustment member includes a first adjustment line and a second driver configured to supply the first adjustment line with a second predetermined voltage so that the first adjustment member adjusts the offset component.

43. The detector according to claim 42, further comprising a first pad, when the first driver supplies the detection member with the first predetermined voltage through a plurality of selection lines, configured to bundle each predetermined number of the plurality of

selection lines and a second pad, independent from the first pad, configured to connect the second driver to the first adjustment line.

44. The detector according to claim 1, further comprising a reset element configured to reset the integration amplifier, and a processor configured to sample the first charge amplified by the integration amplifier at a first timing after a release of a first reset by the reset element and at a second timing between the first timing and a second reset by the reset element.

45. The detector according to claim 44, wherein the first adjustment member includes a first adjustment line and a second driver configured to start to supply the first adjustment line with a second predetermined voltage between the first timing and the second timing so that the first adjustment member adjusts the offset component.

46. The detector according to claim 45, wherein the second driver terminates the supply of the second predetermined voltage between the second timing and a next of the first timing.

47. The detector according to claim 44, wherein the first driver supplies the detection member with the first predetermined voltage in a predetermined period between the first timing and the second timing.

48. The detector according to claim 46, wherein the first driver supplies the detection member with the first predetermined voltage in a predetermined period between the first timing and the termination by the second driver.

49. The detector according to claim 29, wherein the second adjustment member includes a second adjustment line and a third driver configured to supply the second adjustment line with a third predetermined voltage so that the second adjustment member reduces the second charge.

50. The detector according to claim 49, wherein the third driver supplies the second adjustment line with the third predetermined voltage in a substantially same period as the supply of the first predetermined voltage by the first driver.

51. A radiodiagnosis apparatus for obtaining a radiograph, comprising:

a radiation generator configured to generate a radiation;

a radiation detector configured to detect the radiation generated by the radiation generator, the radiation detector including,

a detection member including a plurality of pixels and configured to generate a charge,

a driver configured to supply the detection member with a predetermined voltage so that the detection member generates the charge,

an integration amplifier configured to amplify the charge generated from the detection member and output the amplified charge as a detection signal, and

an adjustment member provided in between the detection member and the integration amplifier, and configured to adjust an offset component included in the charge to be amplified by the integration amplifier;

a memory configured to store a first of the detection signal obtained without the radiation generated by the radiation generator;

a processor configured to obtain a difference signal between the first detection signal stored in the memory and a second of the detection signal obtained when the radiation generator generates the radiation; and

a display configured to display an image based on the detection signal and the difference signal.

52. A radiation detector, comprising:

a detection member including a plurality of pixels and configured to generate a first charge;

a first driver configured to supply the detection member with a first predetermined voltage so that the detection member generates the first charge;

an integration amplifier configured to amplify the first charge generated from the detection member;

a first adjustment member, provided in between the detection member and the integration amplifier, configured to adjust an offset component included in the first charge to be amplified by the integration amplifier; and

a second driver configured to supply the first adjustment member with a second predetermined voltage so that the first adjustment member adjusts the offset component.